WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a Si substrate; and

a resistance element formed on said Si substrate,

said resistance pattern comprising:

a first resistance pattern provided on said substrate at a first level; and

a second resistance pattern provided adjacent to said second resistance pattern at a second level lower than said first level, said second resistance pattern being connected in series to said first resistance pattern,

said second resistance pattern having an edge defined by said first resistance pattern.

2. A semiconductor device as claimed in claim 1, wherein said resistance element further includes an

interlayer insulation pattern underneath said first resistance pattern with a shape in conformity with a shape of said first resistance pattern, said second resistance pattern being provided at a level lower than said interlayer insulation pattern.

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3. A semiconductor device as claimed in claim 1, wherein said first resistance pattern includes a polysilicon pattern and a polycide region formed on said polysilicon pattern, said semiconductor device further comprising a MOS transistor having a polysilicon gate electrode having a composition substantially identical with a composition of said polysilicon pattern.

4. A semiconductor device as claimed in claim 1, wherein said first resistance pattern and said second resistance pattern have a substantially identical resistance.

5. A semiconductor device as claimed in claim 3, wherein said second resistance pattern is formed in said Si substrate in the form of a salicide region defined by said first resistance pattern.

6. A semiconductor device as claimed in claim 5, wherein said Si substrate includes an impurity element with a concentration level such that a parasitic MOS transistor, formed of said first resistance pattern acting as a gate electrode and a pair of said second resistance patterns at both lateral side of said first resistance pattern acting as source and drain regions, has a threshold voltage larger than a supply voltage used in said semiconductor device.

7. A semiconductor device as claimed in claim 1, wherein said second resistance pattern is formed on a device isolation film covering said substrate, said second resistance pattern including a first polysilicon

pattern provided on said insulation film and a salicide region formed on a surface part of said first polysilicon pattern defined by said first resistance pattern.

8. A semiconductor device as claimed in claim 7, wherein said first resistance pattern includes a second polysilicon pattern and a polycide region formed on said second polysilicon pattern, said second polysilicon pattern having an impurity concentration level substantially larger than an impurity concentration level of said first polysilicon pattern.

9. A method of fabricating a semiconductor device, comprising the steps of:

forming a conductive layer on a Si layer;

patterning said conductive layer selectively with respect to said Si layer, to form a conductor pattern;

depositing a metal film on said Si layer such that said conductive film covers said conductor pattern and an exposed part of said Si layer exposed by said conductive film;

annealing said metal film to form a salicide pattern in correspondence to said conductive pattern as a first resistance pattern, said annealing step further forming a salicide pattern in said Si layer in correspondence to said exposed part of said Si layer as a second resistance pattern; and

forming a conductor pattern connecting said first resistance pattern and said second resistance pattern in series.